

# RF Power LDMOS Transistors

## N-Channel Enhancement-Mode Lateral MOSFETs

These 350 W CW RF power transistors are designed for consumer and commercial cooking applications operating in the 915 MHz ISM band.

**Typical Performance:**  $V_{DD} = 48 \text{ Vdc}$ ,  $I_{DQ(A+B)} = 100 \text{ mA}$

Frequency (MHz)	Signal Type	$G_{ps}$ (dB)	PAE (%)	$P_{out}$ (W)
902	CW	20.1	64.1	359
915		20.7	66.9	355
928		20.1	68.1	361

### Load Mismatch/Ruggedness

Frequency (MHz)	Signal Type	VSWR	$P_{in}$ (W)	Test Voltage	Result
915	CW	> 10:1 at all Phase Angles	9.0 (3 dB Overdrive)	48	No Device Degradation

### Features

- Characterized with series equivalent large-signal impedance parameters and common source S-parameters
- Device can be used single-ended or in a push-pull configuration
- Internally input pre-matched for ease of use
- Qualified for operation at 50 Vdc
- Integrated ESD protection
- 150°C case operating temperature
- 225°C die temperature capability

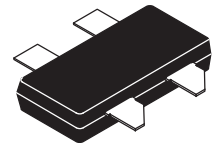
### Typical Applications

- Consumer cooking
- Commercial cooking

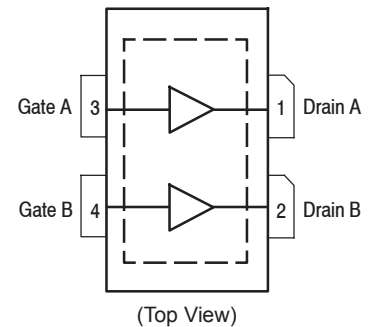
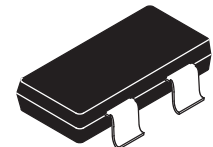
**MHT1002NR3**  
**MHT1002GNR3**

**915 MHz, 350 W CW, 48 V**  
**RF POWER LDMOS TRANSISTOR**  
**FOR CONSUMER AND**  
**COMMERCIAL COOKING**

**OM-780-4L**  
**PLASTIC**  
**MHT1002NR3**



**OM-780G-4L**  
**PLASTIC**  
**MHT1002GNR3**



Note: Exposed backside of the package is the source terminal for the transistors.

**Figure 1. Pin Connections**

**Table 1. Maximum Ratings**

Rating	Symbol	Value	Unit
Drain–Source Voltage	$V_{DS}$	–0.5, +105	Vdc
Gate–Source Voltage	$V_{GS}$	–6.0, +10	Vdc
Operating Voltage	$V_{DD}$	55, +0	Vdc
Storage Temperature Range	$T_{stg}$	–65 to +150	°C
Case Operating Temperature Range	$T_C$	–40 to +150	°C
Operating Junction Temperature Range (1,2)	$T_J$	–40 to +225	°C
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	833 4.17	W W/°C

**Table 2. Thermal Characteristics**

Characteristic	Symbol	Value (2,3)	Unit
Thermal Resistance, Junction to Case Case Temperature $93^\circ\text{C}$ , 350 W CW, 50 Vdc, $I_{DQ} = 100\text{ mA}$ , 915 MHz	$R_{\theta JC}$	0.24	°C/W

**Table 3. ESD Protection Characteristics**

Test Methodology	Class
Human Body Model (per JESD22–A114)	1C, passes 1500 V
Machine Model (per EIA/JESD22–A115)	A, passes 100 V
Charge Device Model (per JESD22–C101)	IV, passes 2000 V

**Table 4. Moisture Sensitivity Level (MSL)**

Test Methodology	Rating	Package Peak Temperature	Unit
Per JESD22–A113, IPC/JEDEC J–STD–020	3	260	°C

**Table 5. Electrical Characteristics** ( $T_A = 25^\circ\text{C}$  unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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**Off Characteristics (4)**

Zero Gate Voltage Drain Leakage Current ( $V_{DS} = 105\text{ Vdc}$ , $V_{GS} = 0\text{ Vdc}$ )	$I_{DSS}$	—	—	10	$\mu\text{Adc}$
Zero Gate Voltage Drain Leakage Current ( $V_{DS} = 48\text{ Vdc}$ , $V_{GS} = 0\text{ Vdc}$ )	$I_{DSS}$	—	—	1	$\mu\text{Adc}$
Gate–Source Leakage Current ( $V_{GS} = 5\text{ Vdc}$ , $V_{DS} = 0\text{ Vdc}$ )	$I_{GSS}$	—	—	1	$\mu\text{Adc}$

**On Characteristics (4)**

Gate Threshold Voltage ( $V_{DS} = 10\text{ Vdc}$ , $I_D = 460\text{ }\mu\text{Adc}$ )	$V_{GS(th)}$	1.3	1.9	2.3	Vdc
Gate Quiescent Voltage ( $V_{DS} = 48\text{ Vdc}$ , $I_{DA} = 860\text{ mAdc}$ )	$V_{GS(Q)}$	—	2.0	—	Vdc
Drain–Source On–Voltage ( $V_{GS} = 10\text{ Vdc}$ , $I_D = 1.3\text{ Adc}$ )	$V_{DS(on)}$	0.1	0.21	0.3	Vdc

**Dynamic Characteristics (5)**

Output Capacitance ( $V_{DS} = 50\text{ Vdc} \pm 30\text{ mV(rms)ac}$ @ 1 MHz, $V_{GS} = 0\text{ Vdc}$ )	$C_{oss}$	—	36.0	—	pF
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1. Continuous use at maximum temperature will affect MTTF.
2. MTTF calculator available at <http://www.freescale.com/rf/calculators>.
3. Refer to AN1955, *Thermal Measurement Methodology of RF Power Amplifiers*. Go to <http://www.freescale.com/rf> and search for AN1955.
4. Each side of device measured separately.
5. Part is input pre-matched. Only output capacitance is measurable.

**Table 6. Typical Performance**

In Freescale Reference Circuit, 50 ohm system,  $V_{DD} = 48$  Vdc,  $I_{DQ(A+B)} = 100$  mA,  $P_{out} = 350$  W, 915 MHz

Characteristic	Symbol	Min	Typ	Max	Unit
Power Gain	$G_{ps}$	—	20.7	—	dB
Power Added Efficiency	PAE	—	66.9	—	%
$P_{out}$ @ 1 dB Compression Point	P1dB	—	387	—	W
$P_{out}$ @ 3 dB Compression Point, CW	P3dB	—	443	—	W
Gain Variation over Temperature (+25°C to +125°C)	$\Delta G$	—	0.04	—	dB/°C
Output Power Variation over Temperature (+25°C to +125°C)	$\Delta P1dB$	—	0.009	—	dB/°C

**Table 7. Load Mismatch/Ruggedness**

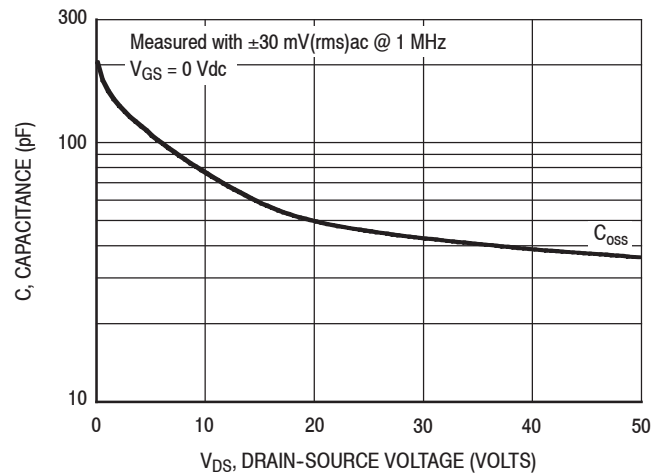
In Freescale Reference Circuit, 50 ohm system,  $I_{DQ(A+B)} = 100$  mA

Frequency (MHz)	Signal Type	VSWR	$P_{in}$ (W)	Test Voltage, $V_{DD}$	Result
915	CW	> 10:1 at all Phase Angles	9.0 (3 dB Overdrive)	48	No Device Degradation

**Table 8. Ordering Information**

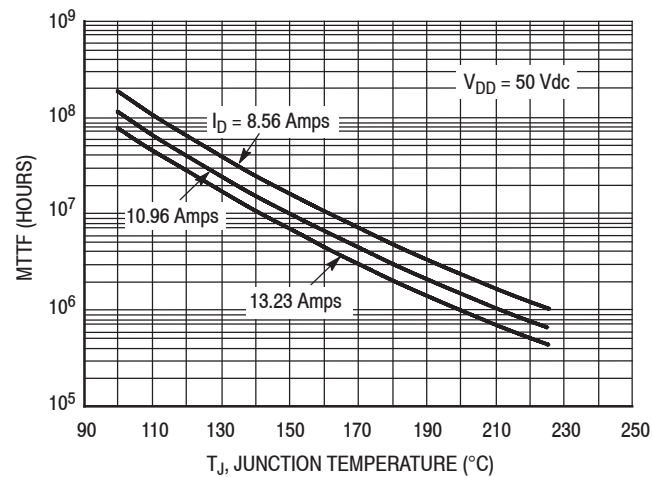
Device	Tape and Reel Information	Package
MHT1002NR3	R3 Suffix = 250 Units, 32 mm Tape Width, 13-inch Reel	OM-780-4L
MHT1002GMR3		OM-780G-4L

## TYPICAL CHARACTERISTICS



**Note:** Each side of device measured separately.

**Figure 2. Capacitance versus Drain-Source Voltage**



**Note:** MTTF value represents the total cumulative operating time under indicated test conditions.

MTTF calculator available at <http://www.freescale.com/rf/calculators>.

**Figure 3. MTTF versus Junction Temperature - CW**

**Table 9. Load Pull Performance — Maximum Power Tuning**

$V_{DD} = 50 \text{ Vdc}$ ,  $I_{DQ(A+B)} = 51 \text{ mA}$ , Pulsed CW, 10  $\mu\text{sec}(\text{on})$ , 10% Duty Cycle

f (MHz)	$Z_{\text{source}}$ ( $\Omega$ )	$Z_{\text{in}}$ ( $\Omega$ )	Max Output Power					
			P1dB					
			$Z_{\text{load}}^{(1)}$ ( $\Omega$ )	Gain (dB)	(dBm)	(W)	$\eta_D$ (%)	PAE (%)
920	$1.37 - j2.19$	$1.46 + j2.62$	$1.18 - j0.65$	19.7	57.3	543	57.9	57.2

f (MHz)	$Z_{\text{source}}$ ( $\Omega$ )	$Z_{\text{in}}$ ( $\Omega$ )	Max Output Power					
			P3dB					
			$Z_{\text{load}}^{(2)}$ ( $\Omega$ )	Gain (dB)	(dBm)	(W)	$\eta_D$ (%)	PAE (%)
920	$1.37 - j2.19$	$1.40 + j2.82$	$1.25 - j0.75$	17.5	57.9	622	57.9	56.8

(1) Load impedance for optimum P1dB power.

(2) Load impedance for optimum P3dB power.

$Z_{\text{source}}$  = Measured impedance presented to the input of the device at the package reference plane.

$Z_{\text{in}}$  = Impedance as measured from gate contact to ground.

$Z_{\text{load}}$  = Measured impedance presented to the output of the device at the package reference plane.

**Table 10. Load Pull Performance — Maximum Power Added Efficiency Tuning**

$V_{DD} = 50 \text{ Vdc}$ ,  $I_{DQ(A+B)} = 51 \text{ mA}$ , Pulsed CW, 10  $\mu\text{sec}(\text{on})$ , 10% Duty Cycle

f (MHz)	$Z_{\text{source}}$ ( $\Omega$ )	$Z_{\text{in}}$ ( $\Omega$ )	Max Power Added Efficiency					
			P1dB					
			$Z_{\text{load}}^{(1)}$ ( $\Omega$ )	Gain (dB)	(dBm)	(W)	$\eta_D$ (%)	PAE (%)
920	$1.37 - j2.19$	$1.32 + j2.64$	$1.17 + j0.14$	21.4	56.2	419	68.3	67.8

f (MHz)	$Z_{\text{source}}$ ( $\Omega$ )	$Z_{\text{in}}$ ( $\Omega$ )	Max Power Added Efficiency					
			P3dB					
			$Z_{\text{load}}^{(2)}$ ( $\Omega$ )	Gain (dB)	(dBm)	(W)	$\eta_D$ (%)	PAE (%)
920	$1.37 - j2.19$	$1.29 + j2.83$	$1.27 + j0.27$	19.5	56.4	441	66.4	65.7

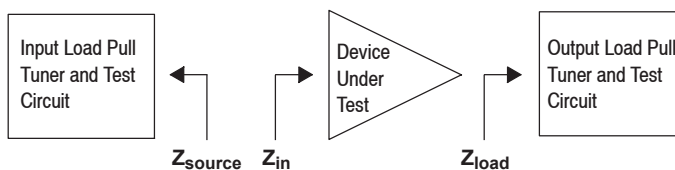
(1) Load impedance for optimum P1dB efficiency.

(2) Load impedance for optimum P3dB efficiency.

$Z_{\text{source}}$  = Measured impedance presented to the input of the device at the package reference plane.

$Z_{\text{in}}$  = Impedance as measured from gate contact to ground.

$Z_{\text{load}}$  = Measured impedance presented to the output of the device at the package reference plane.



## P3dB - TYPICAL LOAD PULL CONTOURS — 920 MHz

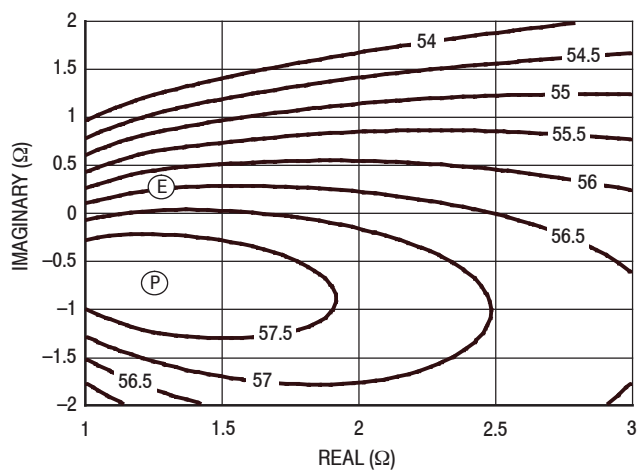


Figure 4. P3dB Load Pull Output Power Contours (dBm)

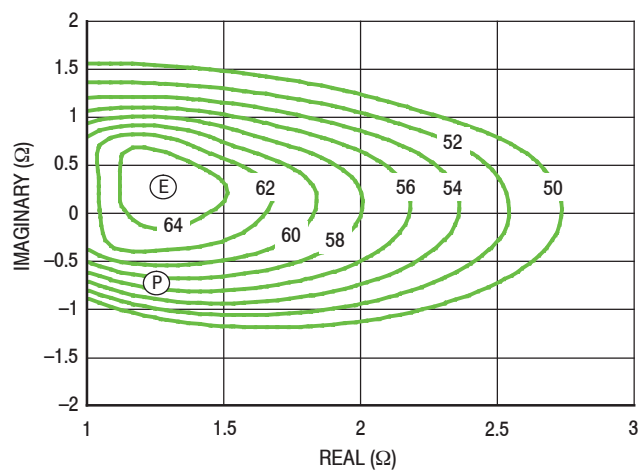


Figure 5. P3dB Load Pull Power Added Efficiency Contours (%)

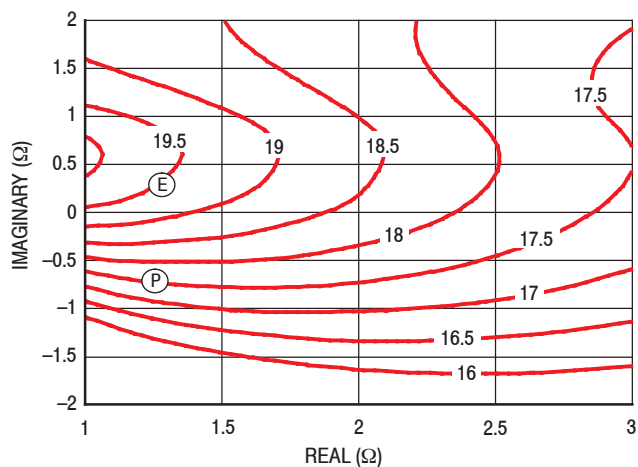


Figure 6. P3dB Load Pull Gain Contours (dB)

**NOTE:** (P) = Maximum Output Power  
(E) = Maximum Power Added Efficiency

— Gain  
— Power Added Efficiency  
— Output Power

## 915 MHz REFERENCE CIRCUIT — 5" × 4"

**Table 11. 915 MHz Performance** (In Freescale Reference Circuit, 50 ohm system)

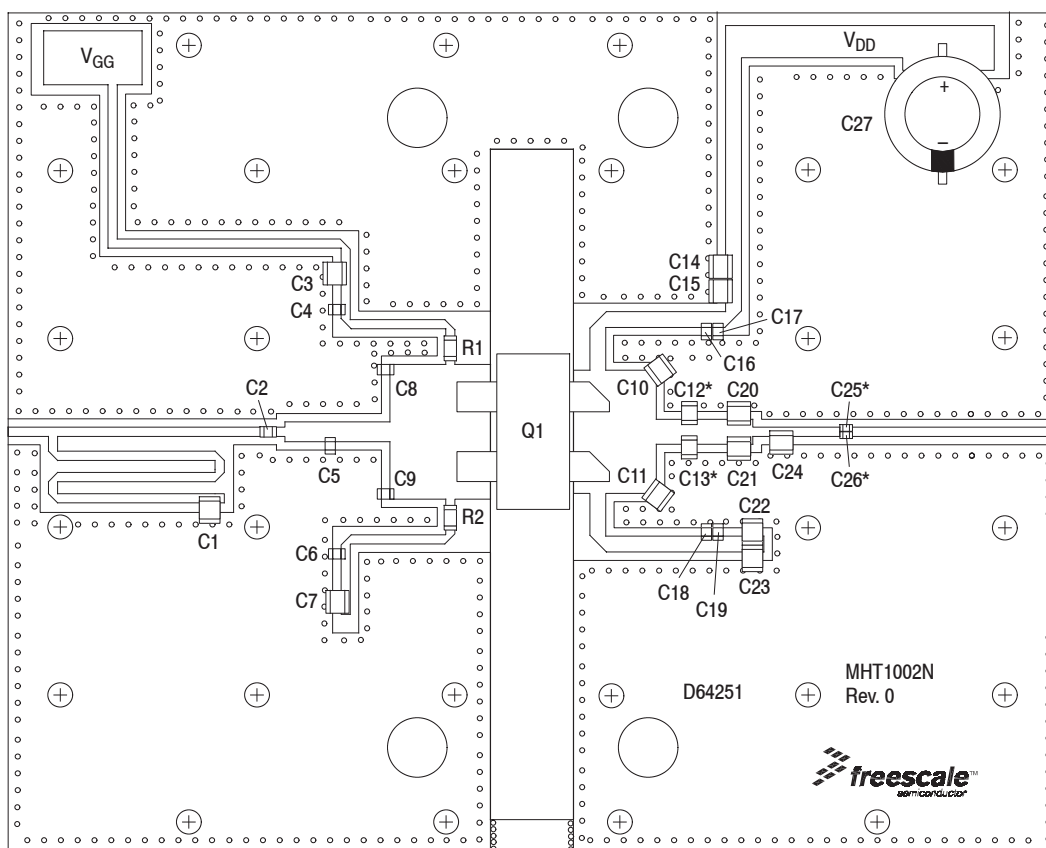
$V_{DD} = 48 \text{ Vdc}$ ,  $I_{DQ(A+B)} = 100 \text{ mA}$ ,  $T_C = 25^\circ\text{C}$

Frequency (MHz)	$P_{in}$ (W)	$G_{ps}$ (dB)	$\eta_D$ (%)	PAE (%)	$P_{out}$ (W)
902	3.5	20.1	64.7	64.1	359
915	3.0	20.7	67.5	66.9	355
928	3.5	20.1	68.7	68.1	361

**Table 12. Load Mismatch/Ruggedness** (In Freescale Reference Circuit)

Frequency (MHz)	Signal Type	VSWR	$P_{in}$ (W)	Test Voltage, $V_{DD}$	Result
915	CW	> 10:1 at all Phase Angles	9.0 (3 dB Overdrive)	48	No Device Degradation

## 915 MHz REFERENCE CIRCUIT — 5" x 4"



\*C12, C13, C25 and C26 are mounted vertically.

Figure 7. MHT1002NR3 Reference Circuit Component Layout — 915 MHz

Table 13. MHT1002NR3 Reference Circuit Component Designations and Values — 915 MHz

Part	Description	Part Number	Manufacturer
C1	62 pF Chip Capacitor	ATC100B620JT500XT	ATC
C2, C5	4.7 pF Chip Capacitors	ATC600F4R7BT250XT	ATC
C3, C7, C14, C15, C22, C23	10 $\mu$ F Chip Capacitors	GRM32ER61H106KA12L	Murata
C4, C6, C16, C17, C18, C19	47 pF Chip Capacitors	ATC600F470JT250XT	ATC
C8, C9	3.9 pF Chip Capacitors	ATC600F3R9BT250XT	ATC
C10, C11	12 pF Chip Capacitors	ATC800B120JT500XT	ATC
C12, C13	5.6 pF Chip Capacitors	ATC800B5R6CT500XT	ATC
C20, C21	2.4 pF Chip Capacitors	ATC800B2R4BT500XT	ATC
C24	2.7 pF Chip Capacitor	ATC800B2R7BT500XT	ATC
C25, C26	39 pF Chip Capacitors	ATC600S390JT250XT	ATC
C27	470 $\mu$ F Electrolytic Capacitor	MCGPR63V477M13X26-RH	Multicomp
Q1	RF Power LDMOS Transistor	MHT1002NR3	Freescale
R1, R2	6.2 $\Omega$ , 1/4 W Chip Resistors	CRCW12066R20FKEA	Vishay
PCB	Rogers RO4350B, 0.020", $\epsilon_r = 3.66$	D64251	MTL



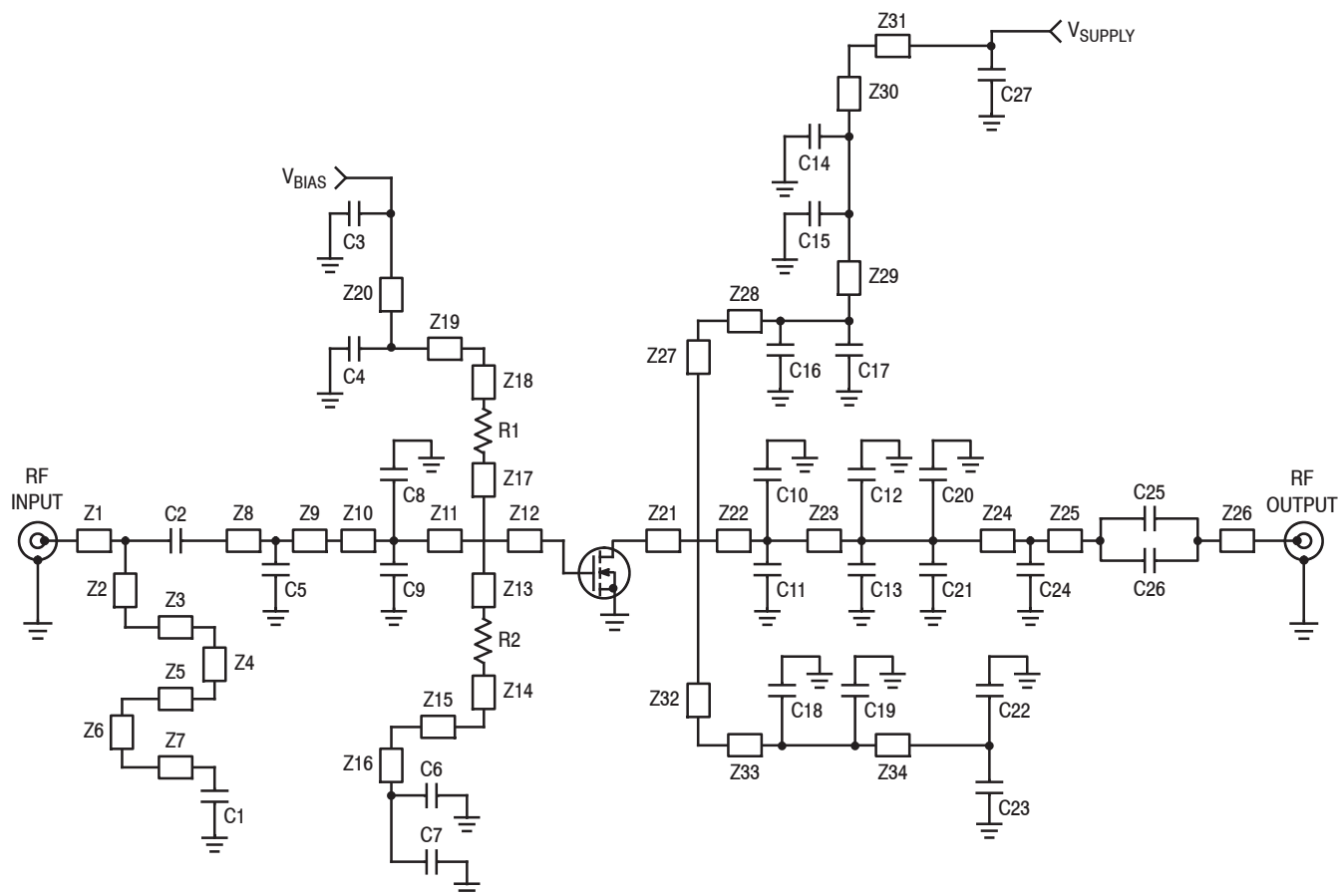


Figure 8. MHT1002NR3 Reference Circuit Schematic — 915 MHz

Table 14. MHT1002NR3 Reference Circuit Microstrips — 915 MHz

Microstrip	Description	Microstrip	Description
Z1	1.218" × 0.044" Microstrip	Z18	0.098" × 0.044" 45° Taper Microstrip
Z2	0.114" × 0.044" 45° Taper Microstrip	Z19	0.489" × 0.044" 45° Taper Microstrip
Z3	0.794" × 0.044" 45° Taper Microstrip	Z20	0.077" × 0.044" 45° Taper Microstrip
Z4	0.101" × 0.044" 45° Taper Microstrip	Z21	0.077" × 0.587" Microstrip
Z5	0.794" × 0.044" 45° Taper Microstrip	Z22	0.241" × 0.587" Microstrip
Z6	0.101" × 0.044" 45° Taper Microstrip	Z23	0.460" × 0.119" Microstrip
Z7	0.794" × 0.044" Microstrip	Z24	0.414" × 0.044" Microstrip
Z8	0.080" × 0.044" Microstrip	Z25	0.223" × 0.044" Microstrip
Z9	0.500" × 0.094" Microstrip	Z26	0.998" × 0.044" Microstrip
Z10	0.010" × 0.642" Microstrip	Z27	0.279" × 0.075" 45° Taper Microstrip
Z11	0.247" × 0.642" Microstrip	Z28	0.643" × 0.075" 45° Taper Microstrip
Z12	0.170" × 0.642" Microstrip	Z29	0.118" × 0.075" Microstrip
Z13	0.044" × 0.050" Microstrip	Z30	1.118" × 0.075" Microstrip
Z14	0.098" × 0.044" 45° Taper Microstrip	Z31	0.769" × 0.153" Microstrip
Z15	0.489" × 0.044" 45° Taper Microstrip	Z32	0.279" × 0.075" 45° Taper Microstrip
Z16	0.331" × 0.044" Microstrip	Z33	0.643" × 0.075" Microstrip
Z17	0.044" × 0.050" Microstrip	Z34	0.094" × 0.075" Microstrip

## TYPICAL CHARACTERISTICS — 915 MHz REFERENCE CIRCUIT

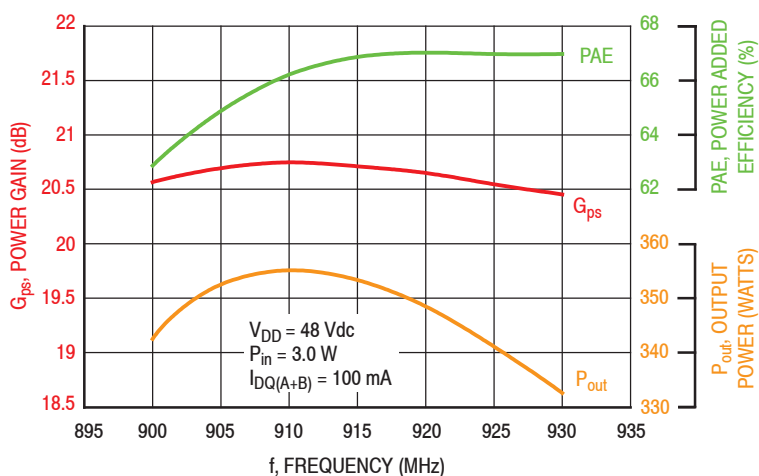


Figure 9. Power Gain, Power Added Efficiency and Output Power versus Frequency at a Constant Input Power

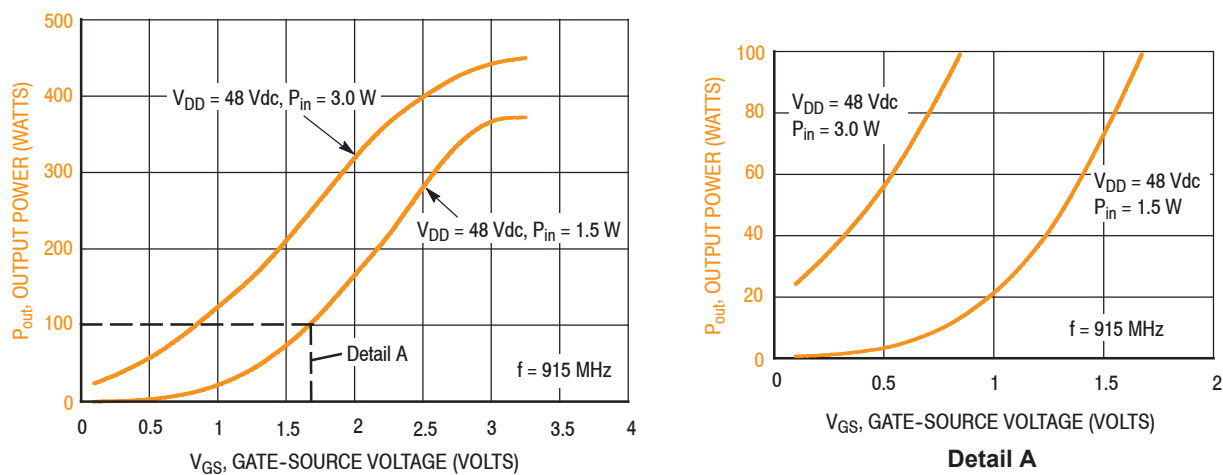


Figure 10. Output Power versus Gate-Source Voltage

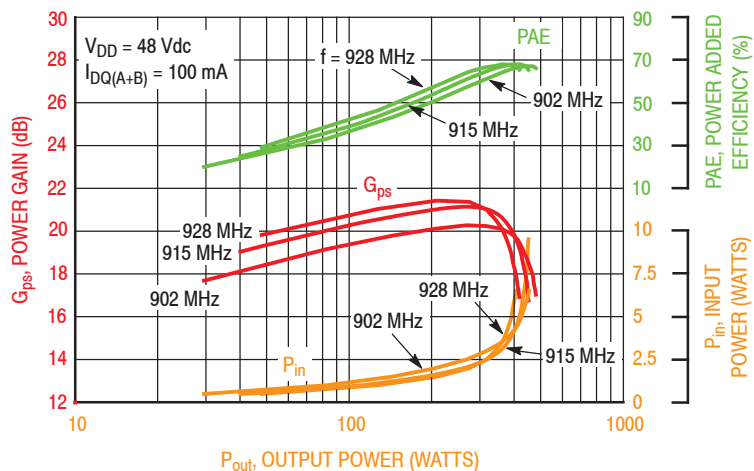
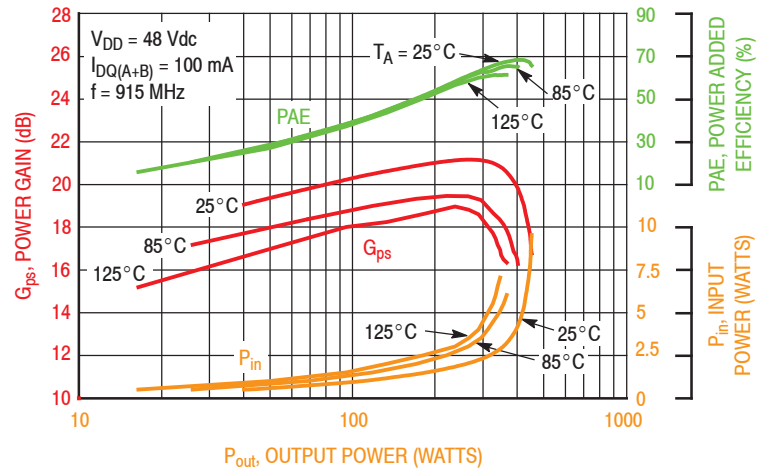


Figure 11. Power Gain, Power Added Efficiency and Input Power versus Output Power and Frequency

## TYPICAL CHARACTERISTICS — 915 MHz REFERENCE CIRCUIT



**Figure 12. Power Gain, Power Added Efficiency and Input Power versus Output Power and Temperature**

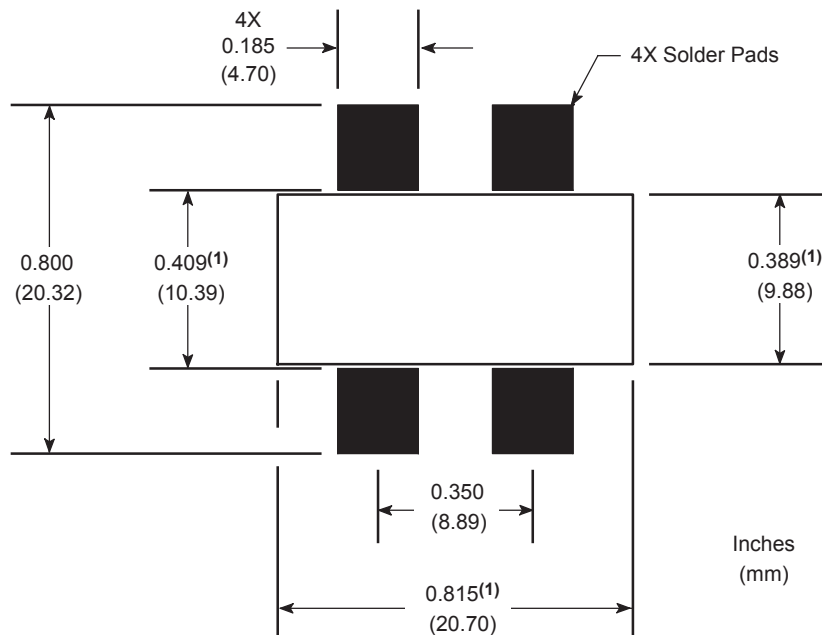


Figure 13. PCB Pad Layout for OM-780-4L

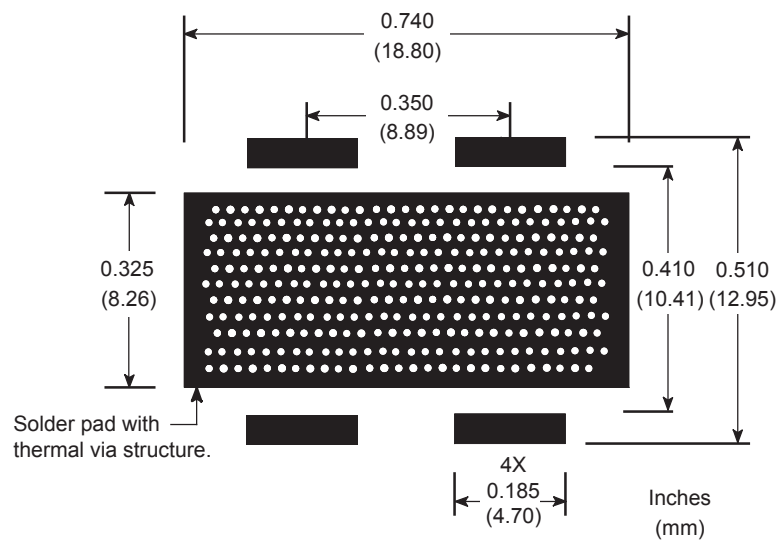


Figure 14. PCB Pad Layout for OM-780G-4L

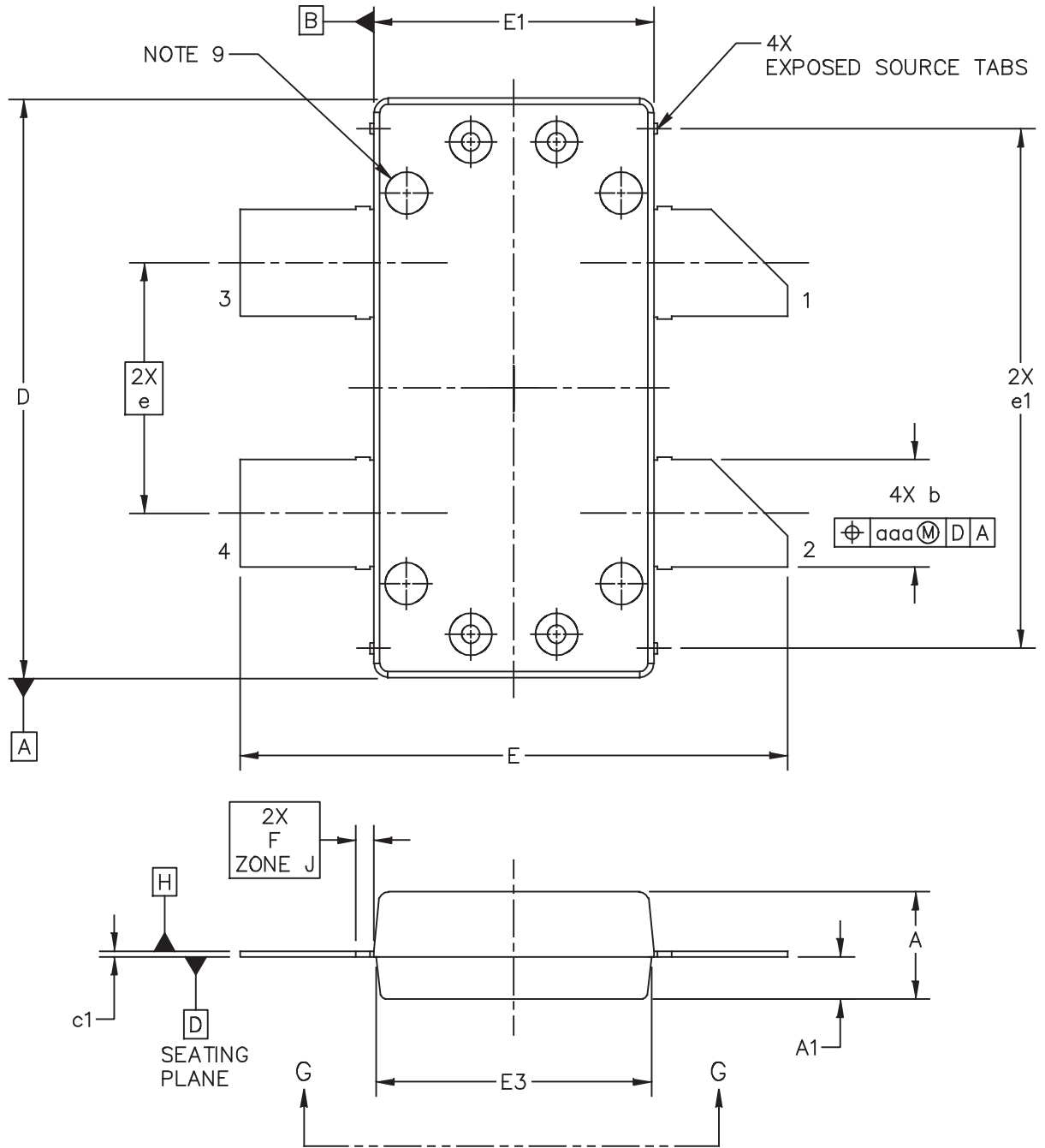


Figure 15. Product Marking — OM-780-4L



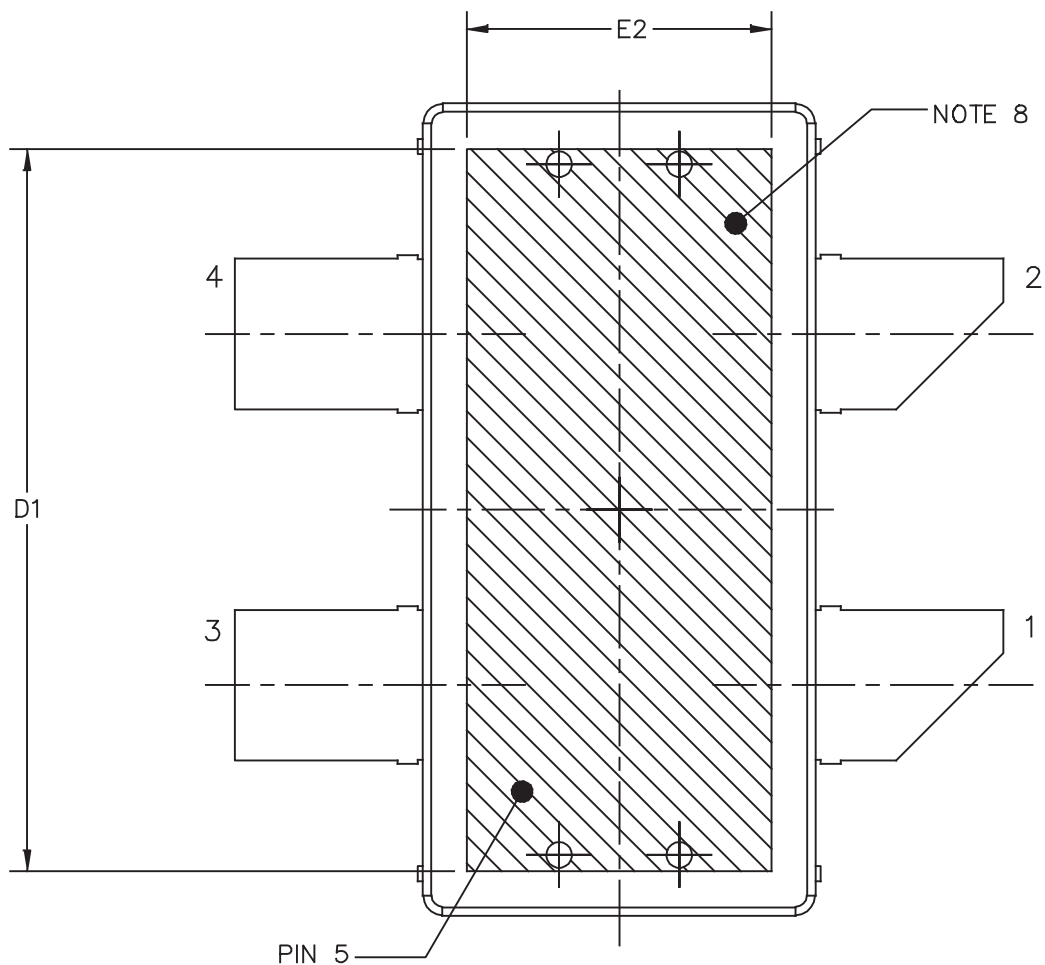
Figure 16. Product Marking — OM-780G-4L

# PACKAGE DIMENSIONS



© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.		MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE
TITLE: OM780-4 STRAIGHT LEAD		DOCUMENT NO: 98ASA10833D	REV: A
		CASE NUMBER: 2023-02	10 FEB 2010
		STANDARD: NON-JEDEC	

MHT1002NR3 MHT1002GNR3



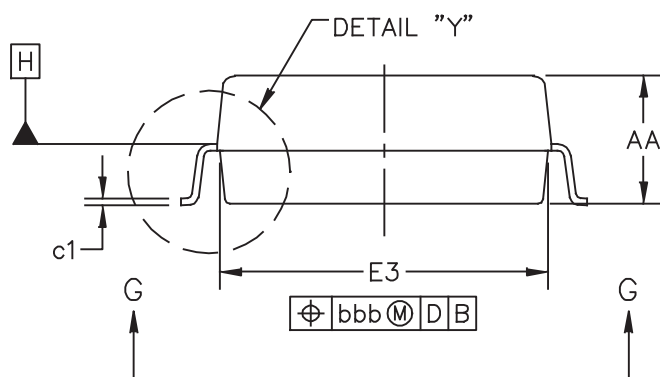
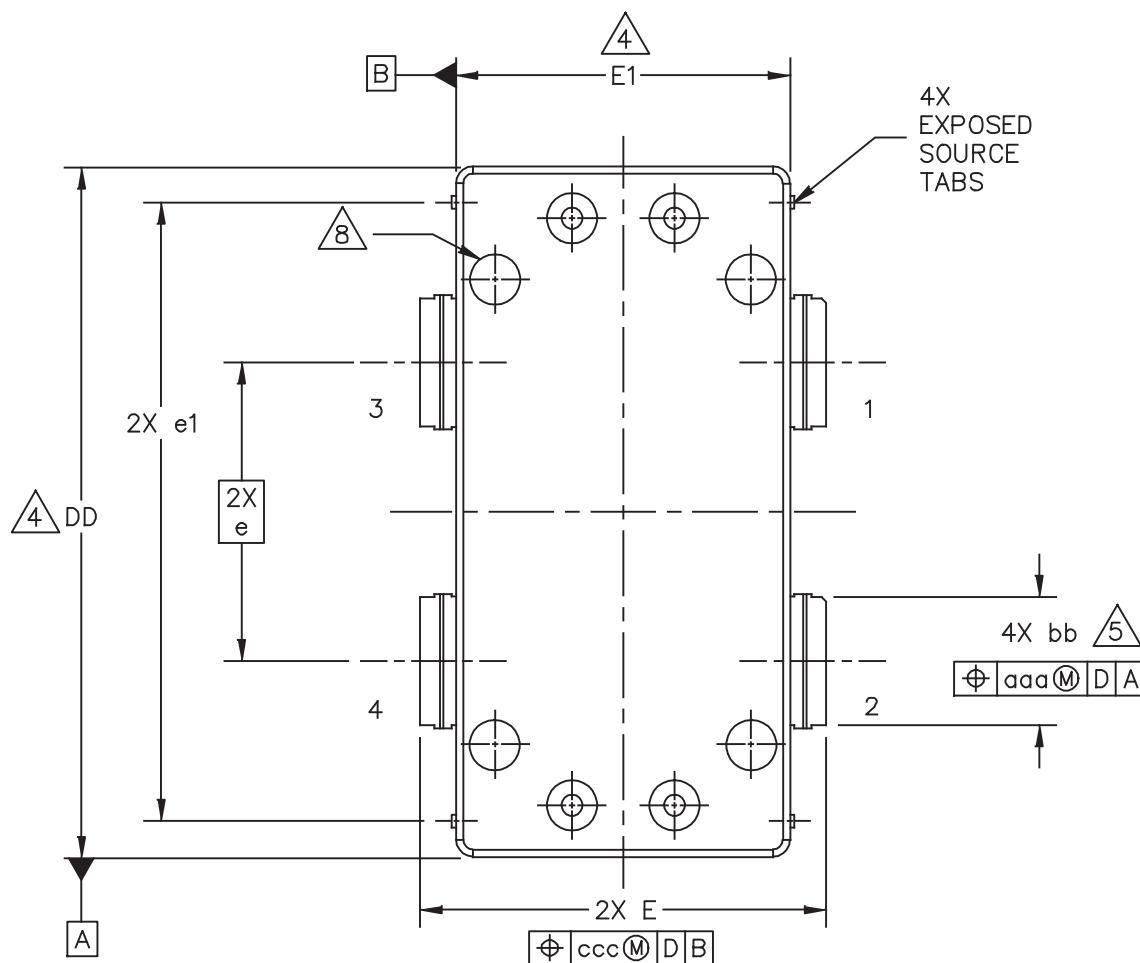
BOTTOM VIEW  
VIEW G-G

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TITLE: OM780-4 STRAIGHT LEAD		DOCUMENT NO: 98ASA10833D	REV: A
		CASE NUMBER: 2023-02	10 FEB 2010
		STANDARD: NON-JEDEC	

NOTES:

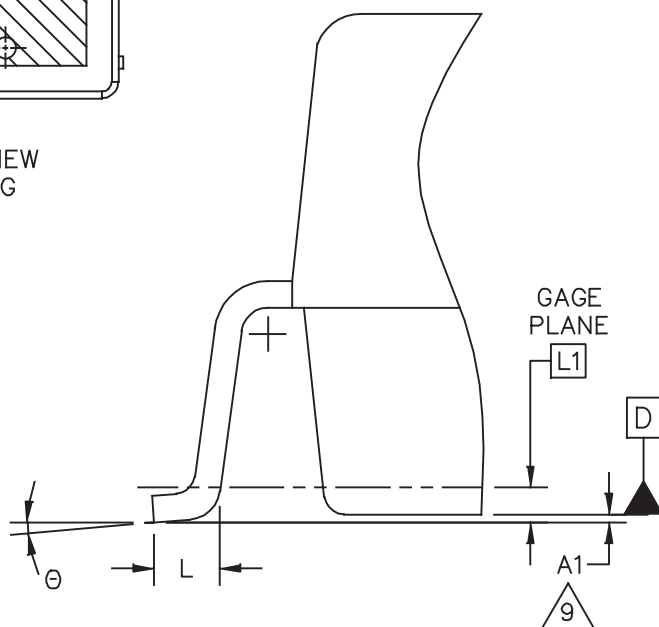
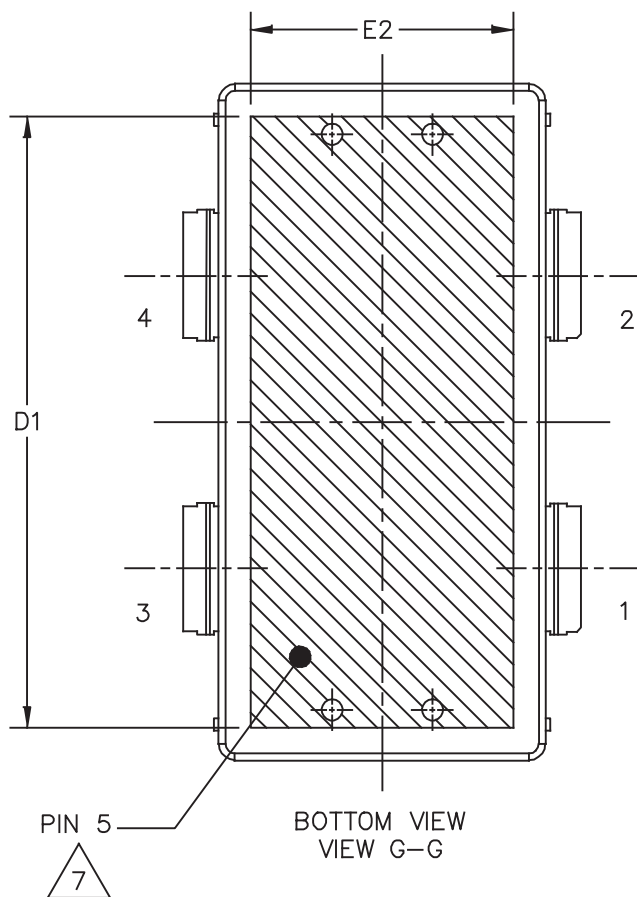
1. CONTROLLING DIMENSION: INCH
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994.
3. DATUM PLANE -H- IS LOCATED AT TOP OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE TOP OF THE PARTING LINE.
4. DIMENSIONS "D" AND "E1" DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS .006 PER SIDE. DIMENSIONS "D AND "E1" DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-.
5. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .005 TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. DATUMS -A- AND -B- TO BE DETERMINED AT DATUM PLANE -H-.
7. DIMENSION A1 APPLIES WITHIN ZONE "J" ONLY.
8. HATCHING REPRESENTS THE EXPOSED AREA OF THE HEAT SLUG. THE DIMENSIONS D1 AND E2 REPRESENT THE VALUES BETWEEN THE TWO OPPOSITE POINTS ALONG THE EDGES OF EXPOSED AREA OF HEAT SLUG.
9. DIMPLED HOLE REPRESENTS INPUT SIDE.

INCH			MILLIMETER		INCH			MILLIMETER	
DIM	MIN	MAX	MIN	MAX	DIM	MIN	MAX	MIN	MAX
A	0.148	.152	3.76	3.86	b	.147	.153	3.73	3.89
A1	.059	.065	1.50	1.65	c1	.007	.011	0.18	0.28
D	.808	.812	20.52	20.62	e	.350 BSC		8.89 BSC	
D1	.720	----	18.29	----	e1	.721	.729	18.31	18.52
E	.762	.770	19.36	19.56	aaa	.004		0.10	
E1	.390	.394	9.91	10.01					
E2	.306	----	7.77	----					
E3	.383	.387	9.72	9.83					
F	.025 BSC		0.635 BSC						
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TITLE:  OM780—4 STRAIGHT LEAD					DOCUMENT NO: 98ASA10833D				REV: A
					CASE NUMBER: 2023—02				10 FEB 2010
					STANDARD: NON—JEDEC				



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TITLE:  OM-780G-4L	DOCUMENT NO: 98ASA10834D      REV: D	
	STANDARD: NON-JEDEC	
	14 NOV 2013	





DETAIL "Y"

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TITLE:  OM-780G-4L	DOCUMENT NO: 98ASA10834D		REV: D
	STANDARD: NON-JEDEC		
			14 NOV 2013

NOTES:

1. CONTROLLING DIMENSION: INCH

2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994.

3. DATUM PLANE H IS LOCATED AT TOP OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE TOP OF THE PARTING LINE.

4. DIMENSIONS DD AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS .006 INCH (0.15 MM) PER SIDE. DIMENSIONS DD AND E1 DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.

5. DIMENSION bb DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .005 INCH (0.13 MM) TOTAL IN EXCESS OF THE bb DIMENSION AT MAXIMUM MATERIAL CONDITION.

6. DATUMS A AND B TO BE DETERMINED AT DATUM PLANE H.

7. HATCHING REPRESENTS THE EXPOSED AREA OF THE HEAT SLUG. THE DIMENSIONS D1 AND E2 REPRESENT THE VALUES BETWEEN THE TWO OPPOSITE POINTS ALONG THE EDGES OF EXPOSED AREA OF HEAT SLUG.

8. DIMPLED HOLE REPRESENTS INPUT SIDE.

9. DIMENSION A1 IS MEASURED WITH REFERENCE TO DATUM D. THE POSITIVE VALUE IMPLIES THAT THE BOTTOM OF PACKAGE IS HIGHER THAN THE BOTTOM OF THE LEAD.

DIM	MIN	INCH MAX	MIN	MILLIMETER MAX	DIM	MIN	INCH MAX	MIN	MILLIMETER MAX
AA	.148	.152	3.76	3.86	bb	.147	.153	3.73	3.89
A1	-.002	.002	-0.05	0.05	c1	.007	.011	0.18	0.28
DD	.808	.812	20.52	20.62	e	0.350 BSC		8.89 BSC	
D1	.720	----	18.29	----	e1	.721	.729	18.31	18.52
E	.470	.482	11.94	12.24	θ	0°	8°	0°	8°
E1	.390	.394	9.91	10.01	aaa	.004		0.10	
E2	.306	----	7.77	----	bbb	.006		0.15	
E3	.383	.387	9.73	9.83	ccc	.010		0.25	
L	.018	.024	0.46	0.61					
L1	.010 BSC		0.25 BSC						

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MECHANICAL OUTLINE

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## PRODUCT DOCUMENTATION, SOFTWARE AND TOOLS

Refer to the resources to aid your design process.

### Application Notes

- AN1907: Solder Reflow Attach Method for High Power RF Devices in Over-Molded Plastic Packages
- AN1955: Thermal Measurement Methodology of RF Power Amplifiers

### Engineering Bulletins

- EB212: Using Data Sheet Impedances for RF LDMOS Devices

### Software

- Electromigration MTTF Calculator
- RF High Power Model
- .s2p File

### Development Tools

- Printed Circuit Boards

### To Download Resources Specific to a Given Part Number:

1. Go to <http://www.freescale.com/rf>
2. Search by part number
3. Click part number link
4. Choose the desired resource from the drop down menu

## REVISION HISTORY

The following table summarizes revisions to this document.

Revision	Date	Description
0	Apr. 2015	<ul style="list-style-type: none"><li>• Initial Release of Data Sheet</li></ul>

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